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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
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MOTOROLA INC			EXAMINER		
AUSTIN INT	ELLECTUAL PROPERT ON	Y .	ECKERT II, GEORGE C		
7700 WEST P AUSTIN, TX	ARMER LANE MD: TX: 78729	32/PL02	ART UNIT	PAPER NUMBER	

DATE MAILED: 08/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No. 10/025,292 Applicant(s)

Cavins et al.

Examiner

George C. Eckert II

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	The MAILING DATE of this communication appears of	n the cover she	et with	the correspondence address		
Period f	or Reply					
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.						
- If the p - If NO p - Failure - Any re	period for reply specified above is less than thirty (30) days, a reply within the seriod for reply is specified above, the maximum statutory period will apply an to reply within the set or extended period for reply will, by statute, cause the ply received by the Office later than three months after the mailing date of th patent term adjustment. See 37 CFR 1.704(b).	nd will expire SIX (6) application to become	MONTHS fi ne ABAND(	om the mailing date of this communication.  NED (35 U.S.C. § 133).		
Status				·		
1) 💢	Responsive to communication(s) filed on <u>Jun 12, 20</u>	003		·		
2a) 💢	This action is <b>FINAL</b> . 2b) ☐ This action	on is non-final.				
3) 🗆	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11; 453 O.G. 213.					
Disposi	tion of Claims					
4) 💢	Claim(s) 1-13 and 15-23			is/are pending in the application.		
4	la) Of the above, claim(s)	*		is/are withdrawn from consideration.		
5) 🗆	Claim(s)					
6) 💢	Claim(s) 1-13 and 15-23					
7) 🗆	Claim(s)					
8) 🗆	Claims					
	ition Papers					
9) 🗆	The specification is objected to by the Examiner.					
10) ▼ The drawing(s) filed on <u>Dec 19, 2001</u> is/are a) ▼ accepted or b) □ objected to by the Examiner.						
	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).					
11)	The proposed drawing correction filed on					
If approved, corrected drawings are required in reply to this Office action.						
12)	The oath or declaration is objected to by the Examin	ner.				
Priority under 35 U.S.C. §§ 119 and 120						
13) Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).						
a) All b) Some* c) None of:						
	1. $\square$ Certified copies of the priority documents have	e been receive	d.	•		
	2. Certified copies of the priority documents have been received in Application No					
*0	3. Copies of the certified copies of the priority do application from the International Bures	au (PCT Rule 1	7.2(a)).			
	tee the attached detailed Office action for a list of the					
14) Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).						
a) The translation of the foreign language provisional application has been received.  15) Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.						
Attachment(s)  1) Notice of References Cited (PTO-892)  4) Interview Summary (PTO-413) Paper No(s)						
	otice of Draftsperson's Patent Drawing Review (PTO-948)	5) Notice of Inf	ormal Pater	nt Application (PTO-152)		
3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6) Other:						

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#### **DETAILED ACTION**

#### Response to Amendment

1. Applicant's response dated June 12, 2003 in which claim 1 was amended and claim 14 canceled has been entered of record.

### Claim Objections

2. Objection to claim 1 based on informalities is withdrawn based on applicant's amendment.

## Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- (e) the invention was described in-
- (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
- (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).
- 3. Claims 1, 2, 7-11, 13, 15-19 and 23 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by US 6,438,030 to Hu et al. The disclosure of Hu et al. teaches all the limitations of

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claims 1, 2, 7-11, 13-19 and 23. It is noted that the instant specification at page 8, line 22 to page 23, line 10 matches the disclosure of Hu et al. at column 3, line 64 to column 11, line 13.

Moreover, the instant figures 1-11 match figures 1-11 of Hu et al. In these identical disclosures are taught, in each occurrence, the limitations of claims 1, 2, 7-11, 13, 15-19 and 23.

4. Claims 11-13, 15 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,143,607 to Chi. Chi teaches, with reference to figures 3, 7 and 11-13, a semiconductor device having a non-volatile memory (NVM) array including rows and columns of memory cells comprising:

a well region 1101 formed within a semiconductor substrate 1103;

a column of memory cells (fig. 7) wherein each memory cell comprises:

a source region 1107 and a drain region 1105 positioned within the well region, wherein each source region is electrically coupled to the well region (note that the source 1107 and well 1101 are the same conductivity);

a tunnel dielectric layer 1201 formed over the substrate;

a charge storage layer 1203 formed over the tunnel dielectric, wherein the charge storage layer comprises discrete storage elements;

a control gate 1303 formed over the charge storage layer;

wordlines (fig. 7), wherein each wordline is electrically coupled to a respective control gate of a memory cell in the column of memory cells; and

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a bitline (fig. 7) electrically coupled to drain regions of each memory cell in column of memory cells.

With regard to claim 12, Chi teach that the devices comprises a blocking layer 1301 of ONO over the charge storage layer (col. 8, lines 1-4). With regard to claim 13, Chi teaches that the charge storage layer comprises polysilicon which is a semiconductor material (col. 7, lines 56-58). With regard to claim 15, Chi teaches that the device is devoid of conductive source lines that electrically couple to each source region (col. 6, lines 47-49). With regard to claim 17, Chi teaches that the well region is P-type (fig. 11).

5. Claims 18 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,679,591 to Lin et al. Lin et al. teach, with reference to figure 15A, a semiconductor device comprising:

a semiconductor substrate 12 comprising a first well region 14a and a second well region 14b, wherein the first well region and the second well region are isolated from each other;

a first memory cell formed in the first well region, the first memory cell comprising:

a first source 36a and a first drain 36b within the first well region having a polarity different than that of the first well region 14a;

a first tunnel dielectric layer 21 (fig. 14) formed over the source and drain region;

a first charge storage layer 22a formed over the first tunnel dielectric layer; and

a first control gate formed over the first charge storage layer 28A; and

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a second memory cell formed in the second well region, wherein the second well memory cell comprises the same layout of the first memory cell including source 36a' and wherein the first and second memory cells are electrically coupled via wordline 28A (WL1).

With regard to claim 19, Lin et al. teach that the first and second well regions 14a and b are both P-type.

#### Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 6. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of US 6,005,270 to Noguchi. Lin et al. taught the device of claim 18 as discussed above. However, Lin et al. did not teach that the first charge storage layer was non-conductive and was covered by a blocking layer or that the second charge storage layer comprised nanocrystals.

Noguchi teaches in figure 1 a non-volatile memory device comprising a tunnel insulator 22a, conductive floating gate 32a, and a control gate 33a. Noguchi further teaches that a non-volatile memory device may be formed using either an ONO layer, wherein the nitride layer serves as the non-conductive charge storage layer, or a nanocrystal layer serving as the charge storage

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layer. See Noguchi, col. 14, line 37 - col. 15, line 30, and col. 15, line 51 - col. 16, line 15.

Noguchi provides motivation to form the non-volatile memory device having an ONO (MONOS) structure or a nanocrystal structure in that they are preferred alternatives to a conductive floating gate layer. Noguchi, col. 5, lines 37-51. Lin et al. and Noguchi are combinable as they are from the same field of endeavor which is non-volatile memory devices. As such, it is considered obvious to combine Lin et al. and Noguchi to achieve the device of instant claims 20-22.

#### **Double Patenting**

7. The terminal disclaimer filed on June 12, 2003 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US 6,438,030 has been reviewed and is accepted. The terminal disclaimer has been recorded. The previous double patenting rejection of claims 3-7, 12 and 20-22 is therefore withdrawn.

## Allowable Subject Matter

8. Claims 3-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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#### Response to Arguments

9. Applicant's arguments filed June 12, 2003 have been fully considered but they are not persuasive. Applicant argues that the §102 rejection of claims 1, 2, 8-11, 13, 15-19 and 23 over Hu et al. must fail because the rejection did not point out where the claim limitations were taught by the prior art. Rather, the rejection merely stated that certain sections of the instant specification and the Hu et al. reference were identical. This is purported as error because it is what is claimed that must be evaluated, not a comparison of what is taught. However, this misconstrues the nature of the rejection. That is, the rejection stated that the claims were *clearly* anticipated by Hu et al. For support, the relevant sections of Hu et al. were referenced and compared to the section of the instant specification which supported the rejected claim limitations. And because the sections are *identical*, and because no more can be instantly *claimed* than what is instantly *taught*, the claims were and are considered clearly anticipated.

Applicant further argues the rejection stating that it failed to consider page 1 through page 8, line 21 and page 23, line 11 through page 31 of the instant specification which are not identical to Hu et al. However, the analysis did not fail to consider these pages, they simply were not relevant to the rejection. Instant page 1 through page 8, line 21 cover mostly background considerations while instant page 23, line 11 to page 31 cover limitations not included in the instant claims. As such, that these pages are not identical is irrelevant to the rejection.

Applicant attempts to further support the argument by questioning specifics of the rejection's "blanket statement." Applicant states that Hu et al. fails to teach or suggest a tunnel

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dielectric as required of independent claims 1, 11, 18 and 23. Applicant further states that the instant specification does not discuss a tunnel dielectric until page 24 which is outside the compared range cited in the rejection. These two statements however absolutely ignore not only the teaching of Hu et al. but the instant specification as well. First of all, Hu et al. teach a tunnel dielectric in at least the following locations: col. 5, lines 30, 32 and 58. Secondly, the instant specification, in a verbatim reiteration of the Hu et al. specification, teaches the same tunnel dielectric on page 11, lines 21, 21-22 and page 12, line 16. Because Hu et al. do teach every limitation of the instant claims, applicant's arguments are not persuasive and the rejections are maintained.

Applicant next argues the rejection of claims 11-13, 15 and 17 over Chi stating that Chi fails to teach discrete storage elements because the storage layer 1203 of Chi is continuous.

Applicant provides no citation to Chi to support the allegation and indeed no support could be found by the examiner. Chi teaches the formation of storage layer 1203 in figure 12 and associated text in column 7 lines 55-65. Though Chi does not use the term continuous, Chi does teach that polysilicon is deposited over a tunnel oxide. However, Chi clearly teaches that the polysilicon and tunnel oxide are then patterned to form a floating gate. The definition of floating gate is a gate that is electrically isolated from all other structures. As such, the allegation that Chi's floating gate (or charge storage layer) is continuous is not supported and the rejection is maintained.

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Applicant lastly argues that the rejection of claims 18 and 19 over Lin is in error as Lin does not teach first and second memory cells formed in first and second wells respectively. This again ignores the teaching of the reference. As acknowledged by applicant, Lin teaches wells 14a-c which are isolated from each other and a memory cell formed in well 14a. However, applicant would deny the teaching of Lin's memory cell in well 14b seemingly because the crosssectional views of figures 8-15b show only well 14a. However, these cross-sectional views are merely for explanation of the device and cannot be construed to limit what is clearly shown in figure 15A. Moreover, as explained by Lin, the cross-section shown in figures 8-14 are taken along line 8-8 of figure 7. Note that in figure 7, wells 14b and 14c also include the same structure as well 14a. As such, Lin does teach the formation of two memory cells in separate wells. Applicant also argues that Lin fails to teach coupling the memory cells with a wordline. Applicants's attention is drawn to figures 15A showing wordline 28A which couples the memory cells in wells 14a, 14b, 14c, etc., as well as to figure 7 which shows wordline 28 also coupling memory cells in the same well. In all, applicants arguments are not persuasive and the rejection is maintained.

#### Conclusion

10. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (703) 305-2752.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Eddie Lee can be reached on (703) 308-1690. The fax number is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

GEORGE ECKERT PRIMARY EXAMINER

GCE August 14, 2003